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		Application Number	09/405,618 - (Conf. #9689)
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	09/24/1999
		First Named Inventor	Blomgren, James S.
		Group Art Unit	2123
		Examiner Name	Craig, Dwin M
		Attorney Docket Number	31876.0140
Sheet	2	of	2

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DME		U.S. Patent Application, "Multiple-State Simulator for Non-Binary Logic." Inventors: Blomgren, et al., Ser. No. 09/405,474, filed on 09/24/1999.	
DME		U.S. Patent Application, "Method and Apparatus for a Monitor that Detects and Reports a Status Event to a Database." Inventors: Weber, et al., Ser. No. 09/406,017, filed on 09/24/1999.	
DME		U.S. Patent Application, "Method and Apparatus that Reports Multiple Status Events with a Single Monitor." Inventors: Weber, et al., Ser. No. 09/406,016, filed on 09/24/1999.	
DME		ROZON, C., On the Use of VHDL as a Multi-Valued Logic Simulator, Proceedings, 26th International Symposium on Multiple-Valued Logic, 05/29-31/1999, pages 110-115.	
DME	✓	WOODS, S., Gate-Level Simulation of Digital Circuits Using Multi-Valued Boolean Algebras, Digest of Technical Papers, 1995 IEEE/ACM International Conference on Computer-Aided Design, 09/24-29/1995, pages 413-419.	
DME	✓	UBAR, R., Multi-Valued Simulation of Digital Circuits, 1997 21st International Conference on Microelectronics, 09/14-17/1997, pages 721-24, Vol. 2.	
DME		IEEE Standards Board, IEEE Standard 1076-1993, IEEE Standard VHDL Language Reference Manual, Approved 09/15/1993.	
DME	✓	TAY, J.C. et al., CSL (Part I), Modelling General N-ary, Logical CSPs, Proceedings, Ninth IEEE International Conference on Tools with Artificial Intelligence, 1997, 11/03-08/1997, pages 414-421.	
DME	✓	TAY, J.C. et al. CSL (Part II), A Compiler for LCSP, Proceedings, Ninth IEEE International Conference on Tools with Artificial intelligence, 1997, 11/03-08/1997.	
DME		WERNER, W. and W. MINNICK, User Requirements for Digital Design Verification Simulators, Annual ACM IEEE Design Automation Conference: Proceedings of the Symposium on Design Automation and Microprocessors, 1977, pages 36-43.	

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Examiner Signature		Date Considered	1-4-02
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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